Prediction and Management of Point Defects for Improved Performance of PV Semiconductors (PV-4)

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Scientific Achievement:

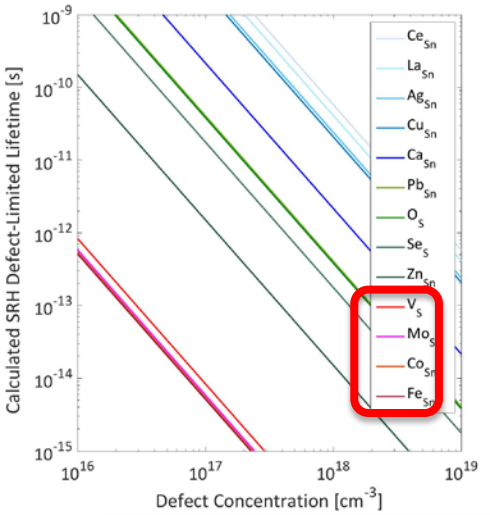
A DFT / SRH model run in collaboration with WUStL[1] identified the most detrimental defects to carrier lifetime in SnS. Carrier lifetimes improved from <100 ps [2] in thin films to >3 ns [3] in bulk crystals with targeted defect engineering.

Significance and Impact:

Device modeling [4] indicates that achieving >1 ns carrier lifetimes in SnS would enable 10+%-efficient devices. We have achieved >3 ns lifetimes in SnS crystals, and are attempting to translate this success to thin films for improved device performance.

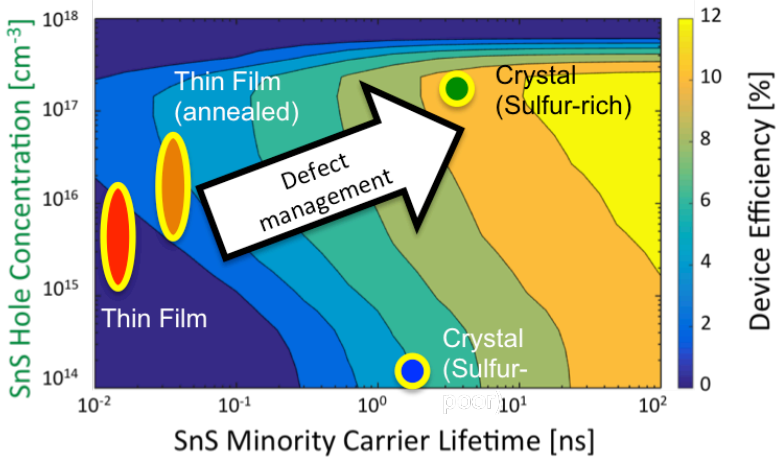
Research Details:

- DFT / SRH model identifies four most detrimental defects: V_S, Mo_{Sn}, Co_{Sn}, and Fe_{Sn}
- Crystal samples grown from feedstocks containing <1 ppb Mo, Co, and Fe
- Crystals grown with S/Sn ratios ranging from 48/52 to 52/48
- Crystals grown with slow (5-day) linear cool-down from melt
- S-rich crystals exhibit improved lifetime (>3 ns) over S-poor crystals (~2 ns), but both show great increases over films (<100 ps)



Right: Simulation (with WUStL) identifies four point defects (in red) as most detrimental to minority-carrier lifetime

Below: Contour plot of calculated device efficiencies vs. SnS carrier content and lifetime. Overlaid with experimental results of higher-lifetime material after defect management.



Publication(s): [1] Polizzotti *et al.*, IEEE PVSC (2016); [2] Jaramillo, R. *et al., J. Appl. Phys.* **119,** 035101 (2016); [3] Polizzotti *et al.,* MRS Fall (2016); [4] Mangan, N. M. *et al. IEEE PVSC* (2014).

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